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1 Optimizing instruction TLB energy using software and hardware techniques

I. Kadayif, A. Sivasubramaniam, M. Kandemir, G. Kandiraju, G. Chen
April 2005 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 10 Issue 2
Publisher: ACM
Full text available: pdf(551.77 KB) Additional Information: full citation, abstract, references, index terms, review

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 58, Citation Count: 0

Power consumption and power density for the Translation Look-aside Buffer (TLB) are important considerations not only in its design, but can have a consequence on cache design as well. After pointing out the importance of instruction TLB (iTLB) power ...

Keywords: Power consumption, cache design, compiler optimization, instruction locality, translation look-aside buffer

2 Entropy-based low power data TLB design

Chinnakrishnan Ballapuram, Kiran Puttaswamy, Gabriel H. Loh, Hsien-Hsin S. Lee
October 2006 CASES '06: Proceedings of the 2006 international conference on Compilers, architecture and synthesis for embedded systems
Publisher: ACM
Full text available: pdf(230.09 KB) Additional Information: full citation, abstract, references, index terms

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The Translation Look-aside Buffer (TLB), a content addressable memory, consumes significant power due to the associative search mechanism it uses in the virtual to physical address translation. Based on our analysis of the TLB accesses, we make two observations. ...

Keywords: entropy, low-power TLB, spatial and temporal locality

3 Surpassing the TLB performance of superpages with less operating system support

Madhusudhan Talluri, Mark D. Hill
December 1994 ACM SIGOPS Operating Systems Review, Volume 28 Issue 5
Publisher: ACM
Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 68, Citation Count: 32

Many commercial microprocessor architectures have added translation lookaside buffer (TLB) support for superpages. Superpages differ from segments because their size must be a power of two multiple of the base page size ...

4 Surpassing the TLB performance of superpages with less operating system support

Madhusudhan Talluri, Mark D. Hill
November 1994 ACM SIGPLAN Notices, Volume 29 Issue 11
Publisher: ACM
Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 68, Citation Count: 32

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5 Surpassing the TLB performance of superpages with less operating system support

Madhusudhan Talluri, Mark D. Hill
November 1994 ASPLOS-VI: Proceedings of the sixth international conference on Architectural support for programming languages and operating systems
Publisher: ACM
Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, cited by, index terms

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Many commercial microprocessor architectures have added translation lookaside buffer (TLB) support for superpages. Superpages differ from segments because their size must be a power of two multiple of the base page size ...

6 Tradeoffs in supporting two page sizes

Madhusudhan Talluri, Shing Kong, Mark D. Hill, David A. Patterson
April 1992 ISCA '92: Proceedings of the 19th annual international symposium on Computer architecture
Publisher: ACM
Full text available: pdf(1.18 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 26, Citation Count: 22

As computer system main memories get larger and processor cycles-per-instruction (CPIs) get smaller, the time spent in handling translation lookaside buffer (TLB) misses could become a performance bottleneck. We explore relieving this bottleneck by (a) ...

7 Tradeoffs in supporting two page sizes

Madhusudhan Talluri, Shing Kong, Mark D. Hill, David A. Patterson
May 1992 ACM SIGARCH Computer Architecture News, Volume 20 Issue 2
Publisher: ACM
Full text available: pdf(1.18 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 26, Citation Count: 22

As computer system main memories get larger and processor cycles-per-instruction (CPIs) get smaller, the time spent in handling translation lookaside buffer (TLB) misses could become a performance bottleneck. We explore relieving this bottleneck by (a) ...

8 Boosting superpage utilization with the shadow memory and the partial-subblock TLB

Cheol Ho Park, JaeWoong Chung, Byeong Hag Seong, YangWoo Roh, Daeyeon Park
May 2000 ICS '00: Proceedings of the 14th international conference on Supercomputing
Publisher: ACM
Full text available: pdf(798.29 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 13, Citation Count: 0

While superpage is an efficient solution to increase TLB reach, its limited flexibility for address mapping is still a hard issue. Our proposed mechanism has been developed for taking advantage of two previous approaches which resolve the issue partially: ...

9 High-bandwidth address translation for multiple-issue processors

Todd M. Austin, Gurindar S. Sohi
May 1996 ISCA '96: Proceedings of the 23rd annual international symposium on Computer architecture
Publisher: ACM
Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 29, Citation Count: 14

In an effort to push the envelope of system performance, microprocessor designs are continually exploiting higher levels of instruction-level parallelism, resulting in increasing bandwidth demands on the address translation mechanism. Most current microprocessor ...

10 High-bandwidth address translation for multiple-issue processors

Todd M. Austin, Gurindar S. Sohi
May 1996 ACM SIGARCH Computer Architecture News, Volume 24 Issue 2
Publisher: ACM
Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 29, Citation Count: 14

In an effort to push the envelope of system performance, microprocessor designs are continually exploiting higher levels of instruction-level parallelism, resulting in increasing bandwidth demands on the address translation mechanism. Most current microprocessor ...

11 Reducing TLB and memory overhead using online superpage promotion

Theodore H. Romer, Wayne H. Ohlrich, Anna R. Karlin, Brian N. Bershad
July 1995 ISCA '95: Proceedings of the 22nd annual international symposium on Computer architecture
Publisher: ACM
Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 32, Citation Count: 26

Modern microprocessors contain small TLBs that maintain a cache of recently used translations. A TLB's *coverage* is the sum of the number of bytes mapped by each entry. Applications with working sets larger than the TLB coverage will perform poorly ...

12 Reducing TLB and memory overhead using online superpage promotion

Theodore H. Romer, Wayne H. Ohlrich, Anna R. Karlin, Brian N. Bershad
May 1995 ACM SIGARCH Computer Architecture News, Volume 23 Issue 2
Publisher: ACM
Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, cited by, index terms

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Modern microprocessors contain small TLBs that maintain a cache of recently used translations. A TLB's *coverage* is the sum of the number of bytes mapped by each entry. Applications with working sets larger than the TLB coverage will perform poorly ...

13

Reducing network latency using subpages in a global memory environment
Hervé A. Jamrozik, Michael J. Feeley, Geoffrey M. Voelker, James Evans, II, Anna R. Karlin, Henry M. Levy, Mary K. Vernon
October 1996 ASPLOS-VII: Proceedings of the seventh international conference on Architectural support for programming languages and operating systems
Publisher: ACM
Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 25, Citation Count: 8

New high-speed networks greatly encourage the use of network memory as a cache for virtual memory and file pages, thereby reducing the need for disk access. Because pages are the fundamental transfer and access units in remote memory systems, page size ...

14 Reducing network latency using subpages in a global memory environment
Hervé A. Jamrozik, Michael J. Feeley, Geoffrey M. Voelker, James Evans, II, Anna R. Karlin, Henry M. Levy, Mary K. Vernon
September 1996 ACM SIGPLAN Notices, Volume 31 Issue 9
Publisher: ACM
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15 Reducing network latency using subpages in a global memory environment
Hervé A. Jamrozik, Michael J. Feeley, Geoffrey M. Voelker, James Evans, II, Anna R. Karlin, Henry M. Levy, Mary K. Vernon
December 1996 ACM SIGOPS Operating Systems Review, Volume 30 Issue 5
Publisher: ACM
Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, cited by, index terms

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New high-speed networks greatly encourage the use of network memory as a cache for virtual memory and file pages, thereby reducing the need for disk access. Because pages are the fundamental transfer and access units in remote memory systems, page size ...

16 Address space sparsity and fine granularity
Jochen Liedtke
September 1994 EW 6: Proceedings of the 6th workshop on ACM SIGOPS European workshop: Matching operating systems to application needs
Publisher: ACM
Full text available: pdf(347.69 KB) Additional Information: full citation, abstract, references

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To fully exploit the potential of large address spaces, e.g. $2^{64}$-byte, the sparsity problem has to be solved in an efficient manner. Current address translation schemes either cause enormous space overhead (page table trees) or do not support ...

17 Address space sparsity and fine granularity
Jochen Liedtke
January 1995 ACM SIGOPS Operating Systems Review, Volume 29 Issue 1
Publisher: ACM

Full text available: pdf(339.76 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 21, Citation Count: 3

To fully exploit the potential of large address spaces, e.g. $2^{64}$-byte, the sparsity problem has to be solved in an efficient manner. Current address translation schemes either cause enormous space overhead (page table trees) or do not support ...

18 Generating physical addresses directly for saving instruction TLB energy

I. Kadayif, A. Sivasubramaniam, M. Kandemir, G. Kandiraju, G. Chen

November 2002 MICRO 35: Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture

Publisher: IEEE Computer Society Press

Full text available: pdf(1.26 MB) Publisher Site Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 15, Citation Count: 3

Power consumption and power density for the Translation Lookaside Buffer (TLB) are important considerations not only in its design, but can have a consequence on cache design as well. This paper embarks on a new philosophy for reducing the number of ...

19 The TLB slice—a low-cost high-speed address translation mechanism

George Taylor, Peter Davies, Michael Farmwald

May 1990 ISCA '90: Proceedings of the 17th annual international symposium on Computer Architecture

Publisher: ACM

Full text available: pdf(731.80 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 53, Citation Count: 19

The MIPS R6000 microprocessor relies on a new type of translation lookaside buffer — called a TLB slice — which is less than one-tenth the size of a conventional TLB and as fast as one multiplexer delay, yet has a high enough ...

20 The TLB slice—a low-cost high-speed address translation mechanism

George Taylor, Peter Davies, Michael Farmwald

June 1990 ACM SIGARCH Computer Architecture News, Volume 18 Issue 3a

Publisher: ACM

Full text available: pdf(731.80 KB) Additional Information: full citation, abstract, references, cited by, index terms

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